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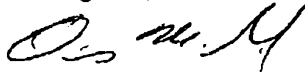
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Dear Examiner Kinkead:

Pursuant to your request in our telephone discussion today, accompanying this facsimile letter are copies of the two (2) references (i.e. EP 0458452 and GB2324919).

If you have any questions, or if you need anything further, please do not hesitate to contact us.

Best regards,



Dennis M. Smid
Encls.

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FIG. 18 is a partial schematic diagram of a circuit having two matched filters and digital processing circuitry that may be used in place of the phase shifter used in FIG. 13.

FIG. 19 is a partial schematic diagram of a circuit having a switched low-pass filter and digital processing circuitry that may be used in place of the phase shifter used in FIG. 13.

As shown in the drawings for purposes of illustration, the present invention relates to 900 MHz-band monolithic frequency converter that can reject an image signal that is as much as 60 dB more powerful than a desired signal.

A time-share mixer circuit includes a mixer, a local oscillator, a switching signal source, and alternating signal means driven by the switching signal. The alternating signal means controls the circuit in such a way that the output alternates rapidly back and forth between an in-phase output signal and a quadrature-phase output signal. In one embodiment the alternating signal means consists of a 90° phase shifter that shifts the phase of the local oscillator signal and a switching element that alternately couples the original and phase-shifted oscillator signals to the mixer. In other embodiments the alternating signal means consists of a clocked inverter in series with one of the ports of the mixer.

A frequency converter according to the invention includes a time-share mixer in combination with an output phase shifter that alternately shifts the phase

of the time-share output signal by 90° . An I-Q modulator according to the invention includes a time-share mixer and an I-Q switching element that alternately couples first and second information signals to the mixer input. Similarly, an I-Q demodulator includes an I-Q switching element and a time-share mixer; the switching element alternately connects the output of the time-share mixer to first and second low-pass filters which in turn provide the demodulated first and second signals.

Circuits embodying the invention are readily adaptable to monolithic construction. The time-share mixer eliminates any need for precisely-matched mixers and amplifiers. The use of a clocked inverter eliminates the need to precisely shift the phase of the local oscillator signal. A frequency converter that embodies the invention can reject an unwanted image signal that is as much as 60 dB stronger than a desired signal.

Turning now to the drawings, a time-share mixer circuit embodying the invention is shown conceptually in FIG. 4. The circuit receives an input signal at an input port 101 and provides a time-share output signal at an output port 103. The circuit includes a mixer 105 having a primary input port 107, an oscillator input port 109, and an output port 111. A local oscillator 113 provides an initial oscillator signal. A switching signal source 115 provides a switching signal. An alternating signal means 117 is responsive to the switching signal to cause the time-share output signal to alternate between an in-phase output signal and a quadrature-phase output signal. The in-phase output signal is that output signal which the mixer would provide if the input signal were applied to the primary input port and the initial oscillator signal were applied to the oscillator input port. The quadrature-phase output signal is that output signal which the mixer would provide if the input signal were provided to the primary input port and the initial oscillator signal were phase-shifted by 90° and then applied to the oscillator input port.

The switching signal is also used by external components, as will be described presently, and is provided for this purpose at a switch signal output port 119.

5 FIG. 5A illustrates a particular embodiment of a time-share mixer circuit as conceptually described above. In this embodiment the input signal at the input port 101 is applied to a primary input port 121 of a mixer 123. The time-share output signal at the output port 103 is provided by an output port 125 of the mixer 123. A local oscillator 127 provides an initial oscillator signal. A switching
10 signal source 129 provides a switching signal. An alternating signal means 131 is realized as a phase shifter 133 and a switching element 135. The phase shifter 133 shifts the phase of the initial oscillator signal by 90° to provide a phase-shifted oscillator signal. The switching element 135 is responsive to the switching signal to alternately couple the initial oscillator signal and the phase-shifted oscillator
15 signal to an oscillator port 137 of the mixer 123.

The switching element 135 is shown for illustrative purposes as a mechanical switch contact. However, it will be apparent that a switching transistor or some other electronic switching element of a kind known to those
20 skilled in the art would normally be used rather than a mechanical switch in this and the other embodiments described herein.

The phase shifter 133 is shown as a separate element from the local oscillator 127. Actually there may be two phase shifters, for example one that
25 introduces a phase shift of $+45^\circ$ and one that introduces a phase shift of -45° , so long as the net effect is to provide two local oscillator signals having a phase difference of 90° between them. The phase shifter and oscillator may be combined in a single quadrature oscillator circuit that provides two signals of the same frequency but with a phase difference of 90° .

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The difference between the phases of the two local oscillator signals must be precisely controlled. In some applications this phase difference must be controlled to within one milliradian at a local oscillator frequency in the range of 1 GHz. However, this requirement can be avoided by using a clocked inverter as the alternating signal means. This eliminates the need for two local oscillator signals. The clocked inverter, which is connected in series with one of the mixer ports, is similar to a synchronous rectifier of the kind that either inverts or does not invert an input signal as ordered by a clocking signal. In a synchronous rectifier the clocking signal is of the same phase and frequency as the input signal, resulting in an output that is a succession of half-cycles all of the same polarity. The output has a DC component, which is why the device is called a "rectifier". In contrast, in a clocked inverter as used in the present invention, the clocking signal is not of the same phase and frequency as the input signal and hence there is no DC component in the output.

Of course, the initial oscillator signal may be generated by phase-shifting the local oscillator output by a first phase shift, for example, $+45^\circ$, and the phase-shifted initial oscillator signal may be generated by phase-shifting the local oscillator output by a second phase shift, for example -45° . There must be a net 90° phase difference between the two signals as alternately applied to the oscillator input port. This is illustrated in FIG. 5B. FIG. 5B is similar to FIG. 5A except that the alternating signal means 131 has been replaced by a slightly different alternating signal means 131A. The means 131A includes two phase shifters 133A and 134A, each of which receives the initial oscillator signal from the local oscillator 127. The shifter 133A shifts the phase by a first amount, for example $+45^\circ$, and the shifter 134A shifts the phase by a second amount, for example -45° ; the amounts of these phase shifts are not critical so long as the difference between them is 90° . A switching element 135A alternates between the two phase-shifted local oscillator signals as driven by the switching signal from the signal source 129.

One embodiment of a time-share mixer that uses a clocked inverter is shown in FIG. 6. An input signal is applied to a primary input port 139 of a mixer 141. An initial oscillator signal provided by an oscillator 143 is applied to an oscillator input port 145 of the mixer 141. A clocked inverter 147 has an input port 149 connected to an output port 151 of the mixer 141. A switching signal source 153 provides a switching signal to the clocked inverter 147 through a 2:1 frequency divider 154 and an input port 155. A time-share output signal is provided at an output port 157 of the clocked inverter. As will be explained in more detail presently, the frequency of the local oscillator in this embodiment differs from the frequency f_{LO} of the local oscillator in the embodiment of FIG. 5A by one-half the switching frequency f_c .

The clocked inverter may be connected in series with either of the input ports of the mixer instead of the output port. This is shown in FIGs. 7 and 8. FIG. 7 shows an embodiment in which a clocked inverter 159 is connected between a local oscillator 161 and an oscillator input port 163 of a mixer 165. The input signal at the port 101 is applied to a primary input port 167 of the mixer and the time-share output signal is provided at a mixer output port 169. The clocked inverter receives a switching signal from a source 171 through a 2:1 frequency divider 172.

FIG. 8 shows an embodiment in which a clocked inverter 173 is connected between the input signal at the input port 101 and a primary input port 175 of a mixer 177. An initial oscillator signal provided by an oscillator 179 is applied to an oscillator input port 181 of the mixer 177, and the time-share output signal is provided at a mixer output port 183. The clocked inverter receives a switching signal from a source 185 through a 2:1 frequency divider 186.

The frequency of the oscillators 161 and 179, like that of the oscillator 143, differs from the frequency f_{LO} by $1/2$ the switching frequency f_c .

Using a clocked inverter provides another advantage besides eliminating the need for precision phase shifting of the local oscillator signal. Any power that might leak from the local oscillator back to the mixer input will be at frequencies very different from the range of desired input frequencies even in case of a low first intermediate frequency. Thus, there is less risk of such a power leakage interfering with desired operation of the circuit or with other similar receivers nearby.

Each of the embodiments as described provides an output signal that switches rapidly back and forth between an in-phase signal and a quadrature-phase signal. It may occur that one of these signals is provided for a somewhat longer portion of each switching cycle than the other. In some applications this is undesirable. A time-share circuit that includes a duty-cycle equalizer to correct this problem is shown conceptually in FIG. 9. This view is similar to that shown in FIG. 4 and for convenience components that are similar in both views have been given the same reference numerals and will not be discussed further.

The duty-cycle equalizer includes a duty-cycle signal source 187 that provides a duty-cycle control signal having a frequency that is an even multiple of that of the switching signal and a duty-cycle circuit element 189 responsive to the duty-cycle control signal to alternately enable the in-phase and quadrature-phase output signals for equal periods of time. The timing of the output signals and the duty-cycle control signal for the case in which the frequency of the duty-cycle signal is double that of the switching signal is illustrated in FIG. 10. Presence of the in-phase signal at the output port 103 is indicated by a HI logic level of the bottom trace 191, and presence of the quadrature-phase signal at the output port 103 is indicated by a HI logic level of the middle trace 193. The duty-cycle circuit element 189 is in a conducting state only when the duty-cycle control signal is at a HI logic level. The duty-cycle control signal, shown as the upper trace 195, is timed to be HI during a portion of the time that the in-phase signal is being provided at the output port 103 and during a portion of the time that the

quadrature-phase signal is being provided at the output port 103. So long as each of these output signals is present for at least as long a time as the duty-cycle circuit element is in a conducting state, each output signal will be present at the output port for exactly as long a time as the other.

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For convenience in illustration, the switching signal source 115 and the duty-cycle signal source 187 are shown as separate signal generators. If separate generators are used in an actual implementation, they should be synchronized as indicated by a dotted line 197 extending from one to the other in FIG. 9. Of course, a single oscillator equipped with suitable frequency-dividing circuitry may serve as the source of both signals.

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An I-Q modulator embodying the teachings of the invention is shown in FIG. 11. The modulator includes an I-Q switching element 199 and a time-share mixer circuit of the kind described and illustrated previously. The modulator as illustrated includes a time-share mixer similar to the one shown in FIG. 5A in combination with a duty-cycle equalizer similar to the one shown in FIG. 9, but it will be apparent that one of the other time-share mixers could be used instead and that the duty-cycle equalizer may be omitted if desired. For convenience, components in FIG. 11 that are similar to components in FIGs. 5 and 9 are given the same reference numerals and will not be discussed further except as necessary.

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The I-Q switching element 199, under control of the switching signal provided by the switching signal source 129, provides an input signal to the primary input port 121 of the mixer 123. The switching element 199 alternates back and forth between a first input signal $f_1(t)$ and a second input signal $f_2(t)$. At the same time, the local oscillator signal as applied to the input port 137 of the mixer is alternated back and forth between two signals having the same frequency but differing in phase by 90° . During those times that the switching element 199 couples the first signal $f_1(t)$ to the mixer, the mixer receives the local oscillator signal with no phase shift and provides at its output the in-phase signal, that is, a

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signal with a carrier frequency as provided by the local oscillator and modulated with the first input signal $f_1(t)$. During those times that the switching element 199 couples the second signal $f_2(t)$ to the mixer, the mixer receives the local oscillator signal with a 90° phase shift and provides at its output the quadrature-phase signal, that is, a signal with a carrier frequency as provided by the local oscillator and modulated with the second input signal $f_2(t)$. The mixer output, after passing through the duty-cycle equalizer, is filtered by a bandpass filter 201 to provide the I-Q output signal modulated with both input signals.

10 An I-Q demodulator embodying the teachings of the invention is shown in FIG. 12. The demodulator includes an I-Q switching element 203 in combination with a time-share mixer circuit of the kind described and illustrated previously and a pair of filters 205 and 207. The demodulator as illustrated includes a time-share mixer similar to the one shown in FIG. 5A, but it will be apparent that one of the other time-share mixers could be used instead and that a duty-cycle equalizer may be provided if desired. For convenience, components in FIG. 12 that are similar to components in FIG. 5A are given the same reference numerals and will not be discussed further except as necessary.

20 The I-Q switching element 203, under control of the switching signal, alternately couples the mixer output to the first low-pass filter 205 and to the second low-pass filter 207. During those times that the switching element couples the output to the first low-pass filter, the mixer is receiving the local oscillator signal without phase shift and is demodulating the input signal to provide the in-phase portion. During those times that the switching element couples the output to the second low-pass filter, the mixer is receiving the local oscillator signal with a 90° phase shift and is demodulating the input signal to provide the quadrature portion. The low-pass filters smooth the switched inputs that they receive to provide the first and second signals, respectively, at the filter outputs.

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If the information carried by the first and second input signals has no DC component, then the filters 205 and 207 may optionally be designed not to pass DC. In this event, these filters would, strictly speaking, be termed "bandpass" filters because their frequency response would not extend all the way down to DC whereas a true "low pass" filter has a frequency response that extends to DC. However, in either case the filters perform the smoothing function to provide the demodulated first and second signals.

Using a clocked inverter rather than switching between two local oscillator signals that must be precisely 90° out of phase with each other eliminates the need for the precise phase control of the oscillator signal and the precision that is required of the switching element. Using the clocked inverter requires that the local oscillator frequency f_{LO} be shifted either up or down by an amount equal to one-half the switching frequency f_C . The phasor of this shifted local oscillator frequency rotates relative to the phasor of the original local oscillator frequency f_{LO} by 180° per full cycle of the switching signal f_C . Consider four consecutive half-cycles (that is, two consecutive cycles) of the switching signal. The average phase difference between the shifted and original local oscillator signals in each of the four half cycles will be incrementing by 90° . By assigning an arbitrary reference frame, the four averages can be assigned the values 0° , 90° , 180° , and 270° . Controlling the clocked inverter with a signal having one-half the frequency of the switching signal alternately inverts and does not invert the polarity of the shifted local oscillator signal such that each of the two states (the inverted state and the non-inverter state) lasts for one full cycle of the switching signal. Due to the polarity inversion (the 180° phase shift), during every other cycle of the switching signal the 180° average phase shift is shifted by another 180° , resulting in a net average phase shift of 0° . Similarly, the 270° average phase shift is shifted by an additional 180° , resulting in a net average phase shift of $270^\circ + 180^\circ = 90^\circ$. Thus the average phase shift between the shifted and original local oscillator frequencies will be 0° , 90° , 0° , and 90° during four consecutive half-cycles of the switching signal f_C .

In summary, the clocked inverter replaces the switching element that switches back and forth between two local oscillator signals that are 90° out of phase with each other with an alternation of phase angles each sweeping over 90° during each half-cycle and with an average phase difference of 90° . Provided a subsequent circuit, such as a bandpass or low pass filter, has the property of averaging its input over an averaging time significantly longer than the period of the switching signal f_c , the result of using the clocked inverter is fully equivalent to the result of switching back and forth between two local oscillator signals 90° out of phase with each other.

An image rejecting frequency converter according to the invention is shown in FIG. 13. This converter includes a time-share mixer similar to the one shown in FIG. 5A in combination with a duty-cycle equalizer similar to the one shown in FIG. 9, but it will be apparent that one of the other time-share mixers could be used instead and that the duty-cycle equalizer may be omitted if desired. For convenience, components in FIG. 13 that are similar to components in FIGs. 5 and 9 are given the same reference numerals and will not be discussed further except as necessary.

In addition to the time-share mixer, the frequency converter includes an output phase shifter 209 and a bandpass filter 211. The output phase shifter 209 receives the time-share mixer output from the port 103 and, responsive to the switching signal, alternately shifts the phase of the time-share output signal by first and second phase shifts, the second phase shift differing from the first by 90 degrees. The bandpass filter receives the phase-shifter output signal from a phase-shifter output port 213 and in turn provides the desired frequency-shifted signal.

The operation of the frequency converter as shown in FIG. 13 may be compared with the prior-art frequency converter shown in FIG. 1. In the circuit of FIG. 1 both the non-phase-shifted and the phase-shifted local oscillator signals are continuously mixed with the input signal in their respective mixers 11 and 13,

but in the circuit of FIG. 13 the single mixer 123 alternates between the non-phase-shifted and the phase-shifted local oscillator signals. In FIG. 1 the second phase shifter 21 is always active on the output of the mixer 13, but in FIG. 13 the output phase shifter 209 switches back and forth in time with the switching of the local oscillator phase shifter. The summing function in FIG. 1 is performed by the summer 19. In FIG. 13, this function is performed inherently by the bandpass filter 211 which averages the two signals that are alternately presented to it. The switching frequency should be significantly higher than the bandwidth of the bandpass filter 211 to assure that the bandpass filter smoothly averages the alternating signals. The elimination of parallel signal paths, parallel mixers, and a summer with parallel inputs eliminates any problem of imbalance in those components and therefore greatly improves the image rejection capability of the circuit.

The bandpass filter 211 is typically included in the first IF amplifier stage, although the filter 211 may be provided as a separate component if desired.

The switching element 135 must have the same gain in both of its positions. However, this requirement may be relaxed if the local oscillator signal is strong enough to drive the mixer 123 into saturation. In this case, the mixer gain is largely independent of the local oscillator signal amplitude as provided to the mixer by the switching element 135.

The output phase shifter 209 must have the same gain for both phase shifts. The exact amount of gain is not critical, but the bandpass filter 211 is canceling the undesired image signal by averaging the alternating components, and perfect cancellation can only be achieved if the time-voltage product of the two components is in balance. Unequal gain between the two phase shifts provided by the phase shifter 209 may be compensated for by adjusting the duty cycle of the switching signal away from 50% as needed.

The duty-cycle element 189 may be placed anywhere between the mixer 123 and the bandpass filter 211. The optimum placement depends on the implementation of the phase shifter 209. Alternatively, the duty-cycle element 189 can be placed between the oscillator signal switching element 135 and the oscillator input port 137 of the mixer 123. The important aspect of the duty-cycle element 189 is that it provides a means for sampling the output of the mixer for a time period that is independent of the ratio of the times for which the two quadrature components are applied to the oscillator input port.

While the time sharing approach taught in the present invention substantially reduces the image rejection problems present in prior art frequency converters, there is one problem specific to the time-sharing concept that is worthy of note. Although the conventional unwanted image signal is suppressed by cancellation, new unwanted image signals are created. The frequencies of these new image signals are given by

$$f_T(m) = f_U \pm mf_C \quad (23)$$

where $f_T(m)$ is the m th image frequency, m is any odd integer, f_U is the frequency of the original unwanted image signal, and f_C is the switching frequency. These unwanted frequencies can be suppressed by selecting a sufficiently high switching frequency f_C .

For example, in a conventional receiver having an intermediate frequency of 1 MHz, the undesired image frequency will be $2f_{IF}$ less than the desired frequency. Thus, if the desired receiver range is 902 to 928 MHz, the unwanted image frequencies will have a range of 900 to 926 MHz. In a receiver embodying a frequency converter according to the invention, a switching frequency $f_C = 200$ MHz will create time-sharing images $f_T(m)$ at least 200 MHz away from f_U . The resulting guard band between the range of the desired frequencies and the nearest of the unwanted image frequencies will be wider than 170 MHz. This guard band is large enough that the time-share image signals can be suppressed by an inexpensive input filter positioned before the mixer.

As has already been mentioned, a preferred embodiment of a frequency converter according to the principles of the invention utilizes a clocked inverter rather than a switched phase shifter in series with the local oscillator. An example of such a frequency converter is shown in FIG 14. A time-share mixer 214,
 5 similar to the one shown in FIG. 6, receives an input at its input port and provides an output at its output port 103 to a phase shifter 216 that is similar to the phase shifter 209 of FIG. 13. The phase shifter 216 in turn is connected to a bandpass filter 218 to provide a frequency-converted signal.

10 For a given input signal having a frequency f_D , the frequency f_{LC} of the oscillator 143 of FIG. 14 will not be the same as would the frequency f_{LO} of the oscillator 127 of FIG. 13 for the same input frequency. From equation (3) above ($f_D = f_{LO} + f_F$) the frequency f_{LO} of the oscillator 127 must be set to $f_{LO} = f_D - f_F$. However, the frequency f_{LC} of the oscillator 143 must differ from this
 15 frequency f_{LO} by an amount equal to $1/2$ the switching frequency f_c . Thus the frequency f_{LC} of the oscillator 143 is given by

$$f_{LC} = f_D - f_F \pm \frac{1}{2}f_c \quad (24)$$

The operation of the circuit of FIG. 14 will now be described in more
 20 detail. Assume, as in (5) above, an input signal of the form

$$D(t) = D\sin(\omega_D t + \phi_D) \quad (25)$$

where D is the amplitude of the desired input signal, ω_D is the angular frequency, and ϕ_D is the phase. The phase angle ϕ_D will be disregarded. The mixer 141 combines the desired input signal $D(t)$ with the local oscillator signal, which may
 25 be expressed as $\cos(\omega_{LC} t)$. The resulting mixer output signal D' includes the term:

$$\frac{1}{2}D\sin(\omega_D - \omega_{LC})t \quad (26)$$

and another term of different frequency that will not survive the subsequent filtering and will therefore be disregarded, as was explained previously with respect to the first mixer of FIG. 1. Thus for present purposes D' may be
 30 expressed as

$$D' = \frac{1}{2}D\sin(\omega_D - \omega_{LC})t \quad (27)$$

Substituting $\omega_D = \omega_{LC} + \omega_{IF}$ and $\omega_{LC} = \omega_{LO} - \omega_C/2$ into (26) yields

$$D' = \frac{1}{2}D\sin(\omega_C/2 + \omega_{IF})t \quad (28)$$

as the signal that is presented to the input port of the clocked inverter 147.

5 The action of the clocked inverter, and the action of the switching at frequency f_C , can be described as chopping its input signal D' by four consecutive chopping pulses P_A , P_B , P_C and P_D . This may be seen by reference to FIG. 15, which shows in vertical alignment two cycles of the switching frequency f_C , one cycle of $f_C/2$, and the four pulses P_A , P_B , P_C and P_D each of which has a frequency $f_C/2$ and a duty cycle of 25%. These four pulses have a DC component, but when
10 multiplying the signal $D' = \frac{1}{2}D\sin(\omega_C/2 + \omega_{IF})t$ by these pulses, the DC component results only in a frequency of $\omega_C/2 + \omega_{IF}$ which will not survive later bandpass filtering. Thus the DC components may be neglected. The AC spectra of the four pulses are given by:

$$15 \quad P_A: (2/(n\pi))\sin(n\pi/4)\cos(n(\omega_C/2 - \pi/4)) \quad (29a)$$

$$P_B: (2/(n\pi))\sin(n\pi/4)\cos(n(\omega_C/2 - 3\pi/4)) \quad (29b)$$

$$P_C: (2/(n\pi))\sin(3n\pi/4)\cos(n(\omega_C/2 - \pi/4)) \quad (29c)$$

$$P_D: (2/(n\pi))\sin(3n\pi/4)\cos(n(\omega_C/2 - 3\pi/4)) \quad (29d)$$

where n is any non-zero positive integer.

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For convenience let $N_{AB} = (2/(n\pi))\sin(n\pi/4)$ and $N_{CD} = (2/(n\pi))\sin(3n\pi/4)$. Then multiplying D' by each of the four pulses and using the trigonometric identity for $\sin x \cos y$ yields:

$$25 \quad D'P_A = D(N_{AB}/4)(\sin((1+n)\omega_C/2 + \omega_{IF}t - n\pi/4) + \sin((1-n)\omega_C/2 + \omega_{IF}t + n\pi/4)) \quad (30a)$$

$$D'P_B = D(N_{AB}/4)(\sin((1+n)\omega_C/2 + \omega_{IF}t - 3n\pi/4) + \sin((1-n)\omega_C/2 + \omega_{IF}t + 3n\pi/4)) \quad (30b)$$

$$D'P_C = D(N_{CD}/4)(\sin((1+n)\omega_C/2 + \omega_{IF}t - n\pi/4) + \sin((1-n)\omega_C/2 + \omega_{IF}t + n\pi/4)) \quad (30c)$$

$$30 \quad D'P_D = D(N_{CD}/4)(\sin((1+n)\omega_C/2 + \omega_{IF}t - 3n\pi/4) + \sin((1-n)\omega_C/2 + \omega_{IF}t + 3n\pi/4)) \quad (30d)$$

Components of these four products that have a frequency ω_{IF} , which are the only components that will survive bandpass filtering centered on that frequency, only exist for $n=1$, in which case $N_{AB} = N_{CD} = (2/\pi)\sin(\pi/4)$. Thus:

$$D'P_A = D'P_C = D(N_{AB}/4)\sin(\omega_{IF}t + \pi/4) \quad (31)$$

5 and

$$D'P_B = D'P_D = D(N_{AB}/4)\sin(\omega_{IF}t + 3\pi/4). \quad (32)$$

The first two signals $D'P_A$ and $D'P_C$ occur in the first half of the cycle of the switching signal f_C and thus these two signals pass through the clocked inverter with no phase shift. The other two signals $D'P_B$ and $D'P_D$ occur in the second half cycle of the switching signal and therefore are phase shifted by 90° , resulting in the following expression for each of the last two after passing through the clocked inverter:

$$D''P_B = D''P_D = D(N_{AB}/4)\sin(\omega_{IF}t + 3\pi/4 - \pi/2) = D(N_{AB}/4)\sin(\omega_{IF}t - \pi/4) \quad (33)$$

All four signals are present in the output. Their sum is:

$$15 \quad D'P_A + D''P_B + D'P_C + D''P_D = D(N_{AB}/2)(\sin(\omega_{IF}t + \pi/4) + \sin(\omega_{IF}t - \pi/4)) \quad (34)$$

or

$$D'P_A + D''P_B + D'P_C + D''P_D = (D/\pi)\sin(\omega_{IF}t). \quad (35)$$

Thus, the desired input signal with angular frequency ω_D has been converted to an intermediate frequency with angular frequency ω_{IF} .

Similar reasoning shows that the undesired image signal will be cancelled.

Just as using the switched phase shifter in conjunction with the local oscillator 127 introduced an undesired new time-share image frequency in the embodiment of FIG. 13, so the clocked inverter also introduces new undesirable time-share image frequencies. The clocked inverter introduces the same image frequencies as does the circuit of FIG. 13. In addition to those image frequencies, the clocked inverter introduces a set of image frequencies $f_T(q)$ which are given by

$$30 \quad f_T(q) = f_D \pm qf_C \quad (36)$$

where q is an even non-zero integer. These new time-sharing image frequencies can also be suppressed by choosing a switching frequency f_c that allows for a sufficient guard band.

5 The frequency converting circuits illustrated in FIGs. 13 and 14 use an analog phase shifter 209. A preferred implementation of such a phase shifter meets at least two conditions. First, the two paths generating the two phase shifts must share the same circuitry as much as possible. This minimizes balance errors due to circuit component mismatches. Second, the implementation must not
10 require a high gain amplifier operating at a wide bandwidth, since one of the reasons for utilizing a time-shared mixer is to avoid such wide-bandwidth, high-gain amplifiers.

 One implementation of a suitable analog phase shifter is shown in FIG. 16.
15 This circuit similar to the one shown in FIG. 13; similar components have the same reference numerals and will not be discussed further. An amplifier 215 receives the time-share mixer output signal from the output port 103 of the time-share mixer. The amplifier 215 provides complementary outputs $+V$ and $-V$ at first and second amplifier outputs 217 and 219, respectively. The first output 217
20 is connected to a resistor 221 which in turn is connected to the output port 213. The second output 219 is connected to two capacitors 223 and 225 which in turn are connected to first and second terminals of a switching element 227. The switching element 227 has a pole connected to the output port 213. The switching element 227 is controlled by the switching signal.

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 The values of the resistor 221 and the capacitors 223 and 225 are chosen to generate two signals with a relative phase shift of 90° . For example, the respective phase shifts may be 45° and 135° . In choosing the values of these components, it should be noted that the capacitors are connected to the resistor
30 only during a fraction p and $(1-p)$ of time, where p is the switching duty cycle (ideally $p=50\%$). An error in the duty cycle would result in a proportional error

in the effective ratio of the two capacitors and hence in the relative phase shifts of the two signals. Of course, the duty cycle could be deliberately adjusted to compensate for any error in the values of the capacitors.

5 A frequency converter which utilizes a second time-share mixer to provide the phase shift is shown in FIG. 17. A first time-share mixer circuit generally 227 receives an input signal at its input port 229 and provides an output at its output port 231. The output port 231 connects through a bandpass filter 233 to an input port 235 of a second time-share mixer circuit generally 237 which serves as a
10 phase shifter. The phase shifter 237 provides an output to a bandpass filter 239 at its output port 241.

 In the embodiment as illustrated, the time-share mixer circuits 228 and 237 are each similar to the embodiment shown in FIG. 5A except that a single
15 switching signal source 243 provides the switching signal for both circuits. The circuit 228 includes a mixer 245 that receives the input signal presented to the input port 229 and provides the output to the output port 231. The mixer 245 has an oscillator input that is alternately connected by a switching element 247 to a
20 local oscillator 249 and to a phase shifter 251 that shifts the phase of the local oscillator by 90°. Similarly the circuit 237 includes a mixer 253 that receives the input signal presented to the input port 235 and provides the output to the output port 241. The mixer 253 has an oscillator input that is alternately connected by a
25 switching element 255 to a local oscillator 257 and to a phase shifter 259 that shifts the phase of the local oscillator by 90°. The switching signal source drives both switching elements 247 and 255.

 In some embodiments a separate switching signal source may be used to drive the switching element 255. This would be the case, for example, if the filter 233 were implemented by a pair of switched filters such as those shown in FIG.
30 18, which will be discussed presently.

The second time-share mixer circuit 237 will be sensitive to an unwanted image frequency in its input. Such an unwanted image frequency could result from an unwanted signal at the input to the first mixer circuit 228. The filter 233 will reject any such unwanted image frequency. The filter 233 may be
5 implemented by, for example, a low-pass filter similar to the filter 277 shown in FIG. 19, which will be discussed presently.

One or both of the time-share mixer circuits 228 and 237 may be replaced with an alternate embodiment such as one of those shown in FIGs. 6, 7 or 8.
10

As noted above, a high switching frequency of, *e.g.*, $f_c = 200\text{MHz}$ is desirable to ensure a sufficient distance between the time-share images and the desired input frequency of the frequency converter. However, the useful information at the output of the phase shifter (209 in FIG. 13) is carried by a
15 signal at an intermediate frequency f_{IF} and therefore can be processed by relatively low frequency circuits such as the bandpass filter 211.

In many applications it would be advantageous to replace the phase shifter 209 and bandpass filter 211 in the circuit of FIG. 13 with more accurate digital
20 signal processing hardware. Digital processing hardware that could process a signal switched at a relatively high frequency such as 200 MHz would draw too much power. Therefore, to take advantage of the capabilities of digital signal processing without excessive power drain, the switching frequency of the signal must be significantly reduced before it is processed by the digital hardware.
25 However, to keep the time-share images away from the desired input frequency, this must be done without reducing the high switching frequency used in the frequency converter circuit. This can be accomplished by filtering the two quadrature components of the time-share mixer output signal separately and replacing the output phase shifter 209 and bandpass filter 211 with digital signal
30 processing circuitry that accomplishes the functions of these components. A circuit that can be used for this purpose is shown in FIG. 18.

FIG. 18 shows a frequency converter that uses a time-share mixer similar to those discussed above. A time-share mixer 261 generally similar to the circuit shown in FIG. 5A is used in the embodiment as illustrated, but it will be apparent that any of the other time-share mixers discussed and illustrated previously could be used instead. An I-Q switching element 263 controlled by the switching signal receives the output signal from the output port of the time-share mixer 261. The I-Q switching element 263 has two outputs, one of which drives a filter 265 and the other of which drives a filter 267. A second I-Q switching element 269, controlled by a switching signal source 271, alternately connects the outputs of each of the filters 265 and 267 to an analog-to-digital converter 273. The output of the A-to-D converter 273 in turn is provided to a digital phase shifter and summer 275.

The filter 265 may be designated the "I" filter and the filter 267 may be designated the "Q" filter. These filters convert the alternating I and Q components at the output 103 of the time-share mixer circuit 261 into continuous I and Q signal streams, respectively. Therefore the frequency of the signal source 271 may be different than that of the switching signal provided at the switching signal output port 119 of the time-share mixer 261. The frequency of the signal source 271 is preferably chosen low enough to allow digital signal processing without excessive power drain.

To maintain a high degree of image rejection, the filters 265 and 267 must pass the I and Q components of the intermediate frequency signal as provided at the output port 103 of the time-share mixer 261 with well-matched phase shift and gain. This will be facilitated if the filters 265 and 267 share as many components as possible. A circuit in which the two filters share most of their components is shown in FIG. 19.

The circuit of FIG. 19 is in many respects similar to the circuit of FIG. 18, and for convenience similar components have been assigned the same reference

numerals in both figures. A low-pass filter circuit generally 277 replaces the I-Q switching elements 263 and 269 and the filters 265 and 267 of FIG. 18. The filter 277 receives the signal from the output port 103 of the time-share mixer 261. The filter 277 comprises a plurality of cascaded RC filter stages and a sample-and-hold element 279. The first such RC filter stage includes a resistor 281 that receives the signal and couples it to an input of an amplifier 283. A switching element 285, driven by the switching signal from the port 119 of the mixer circuit, alternately connects a capacitor 287 and a capacitor 289 to the input of the amplifier 283.

Similarly, the second filter stage includes a resistor 291 that receives the signal from the first filter stage and couples it to an input of an amplifier 293. A switching element 295, driven by the switching signal from the port 119 of the mixer circuit, alternately connects a capacitor 297 and a capacitor 299 to the input of the amplifier 293. The third filter stage includes a resistor 301 that receives the signal from the second filter stage and couples it to an input of an amplifier 303. A switching element 305, driven by the switching signal from the port 119 of the mixer circuit, alternately connects a capacitor 307 and a capacitor 309 to the input of the amplifier 303. The amplifiers are typically emitter or source followers that act as buffers.

The output from the third filter stage is provided to the sample-and-hold element 279 and thence to the A-to-D converter 273. The sample-and-hold element 279 is controlled by the switching signal source 271.

The sample-and-hold 279 has an acquisition aperture shorter than $1/(2f_c)$ but is triggered by a signal provided by the signal source 271 that has a frequency f_s that is chosen to be an odd submultiple of $2f_c$. As a result, samples taken by the sample-and-hold 279 alternate between the quadrature samples taken from the capacitors 287, 297 and 307, and alternate-phase quadrature samples taken from the capacitors 289, 299 and 309. Choosing the frequency f_s of the switching

signal source 271 such that $f_s > f_o + f_{IF}$, where f_o is the stop band edge of the low-pass filter 277, prevents any signal coming out of the low-pass filter from aliasing into the IF signal. Because two samples constitute a single reduced-frequency switching cycle, the switched low-pass filter and sample-and-hold circuit in combination have the effect of reducing the switching frequency as it appears in the output of the sample-and-hold from f_c to a new frequency $f_c' = f_s/2$. In a practical case in which $f_c = 200\text{MHz}$, f_c' could be as low as $< 7\text{ MHz}$.

The signal provided by the sample-and-hold is converted to digital form in the A-to-D converter 273. Once the signal has been digitized, an accurate 90° phase shift between the two quadrature components is easily accomplished using conventional digital techniques, for example in the digital phase shifter and summer 275.

From the foregoing it will be appreciated that the time-share mixer provides a frequency converter having capabilities not heretofore attainable in a monolithic receiver. A frequency converter embodying the principles of the invention can reject an unwanted image signal that is as much as 60 dB more powerful than the desired signal.

Although various specific embodiments of the invention have been described and illustrated, the invention is not to be limited to the specific forms or arrangements of parts so described and illustrated. The invention is limited only by the claims.

CLAIMS

1. A frequency converter for shifting the carrier frequency of an RF signal, the frequency converter comprising:
 - a mixer having a primary input port, an oscillator input port, and an output port;
 - a local oscillator that provides an initial oscillator signal;
 - a switching signal source that provides a switching signal;
 - alternating signal means responsive to the switching signal to cause the time-share output signal to alternate between an in-phase output signal and a quadrature-phase output signal, the in-phase output signal being that output signal which the mixer would provide if the RF signal were applied to the primary input port and the initial oscillator signal were applied to the oscillator input port, the quadrature-phase output signal being that output signal which the mixer would provide if the RF signal were provided to the primary input port and the initial oscillator signal were phase-shifted by 90 degrees and then applied to the oscillator input port; and
 - switched output phase shift means, responsive to the switching signal, for alternately shifting the phase of the time-share output signal by first and second phase shifts differing from one another by 90 degrees to generate two phase-shifted signal components, and for summing the two phase-shifted signal components.
2. The frequency converter of claim 1, wherein the alternating signal means comprises:
 - a phase shifter that shifts the phase of the initial oscillator signal by 90 degrees to provide a phase-shifted oscillator signal; and
 - a switching element, responsive to the switching signal, for alternately coupling the initial oscillator signal and the phase-shifted oscillator signal to the oscillator port of the mixer.

3. The frequency converter of claim 1, wherein the alternating signal means comprises a clocked inverter in series with a port of the mixer.
4. The frequency converter of claim 1 or 3, wherein the RF signal is applied to the primary input port, the initial oscillator signal is applied to the oscillator input port, and the clocked inverter is connected in series with the mixer output port to provide the time-share output signal.
5. The frequency converter of claim 1 or 3, wherein the RF signal is applied to the primary input port of the mixer, the initial oscillator signal is applied to the oscillator input port through the clocked inverter, and the time-share output signal is provided at the mixer output port.
6. The frequency converter of claim 3, wherein the RF signal is applied to the primary input port of the mixer through the clocked inverter, the initial oscillator signal is applied to the oscillator input port, and the time-share output signal is provided at the mixer output port.
7. The frequency converter of any one of claims 1 to 6, additionally comprising a duty-cycle equalizer operative to equalize the in-phase duty cycle with the quadrature-phase duty cycle of the time-share output signal.
8. The frequency converter of any of claims 1 to 7, wherein the switched output phase shift means includes:
 - an output phase shifter, responsive to the switching signal, for alternately shifting the phase of the time-share output signal by first and second phase shifts differing from one another by 90 degrees to generate two phase-shifted signal components; and
 - a bandpass filter for summing the two phase-shifted signal components to generate the desired frequency-shifted signal.

9. The frequency converter of any of claims 1 to 7, wherein the output phase shift means includes:

an in-phase filter;

a quadrature filter;

a first quadrature switching element that receives the time-share output signal and alternately provides said output signal to the in-phase and quadrature filters under control of the switching signal;

an analog-to-digital converter;

a second switching signal source that provides a second switching signal;

a second quadrature switching element controlled by the second switching signal to alternately couple the in-phase and quadrature filters to the analog-to-digital converter; and

a digital phase shifter, coupled to the analog-to-digital converter, that provides the desired frequency-shifted signal.

10. The frequency converter of any of claims 1 to 7, wherein the switched output phase shift means includes:

a low-pass filter stage for filtering the time-share output signal, the low-pass filter stage including a resistor, a first capacitor, a second capacitor, switching means responsive to the switching signal to alternately connect the first capacitor and the second capacitor in series with the resistor, and an output amplifier;

a sample-and-hold circuit that samples the filtered time-share output signal;

an analog-to-digital converter that converts the samples provided by the sample-and-hold circuit into a digital signal; and

a digital phase shifter that alternately shifts the phase of the digital signal by first and second phase shifts, the second phase shift differing from the first by 90 degrees, and thereby provides the desired frequency-shifted

signal.

11. The frequency converter of any of claims 1 to 7, wherein the switched output phase shift means includes:

a filter that filters the time-share output signal from the time-share mixer circuit;

a second mixer having a primary input port that receives the filtered signal from the filter, an oscillator input port, and an output port;

a second local oscillator that provides a second initial oscillator signal; and

second alternating signal means responsive to a switching signal to cause an output signal provided at the second mixer output port to alternate between first and second output signals, the first output signal being that output signal which the second mixer would provide if the second initial oscillator signal were applied to the second mixer oscillator input port, the quadrature-phase output signal being that output signal which the second mixer would provide if the second initial oscillator signal were phase-shifted by 90 degrees and then applied to the second mixer oscillator input port.

12. A frequency converter substantially as herein described with reference to Figs. 13 to 19 of the accompanying drawings.



The
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Claims searched: 1 to 12

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UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H3R (RMB, RMC, RMX, RFMA, RFDX)

Int Cl (Ed.6): H03D 7/00, 7/18

Other: Online: WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	US 4321549 (HANSEN) see figure 2	
A	US 4320531 (DIMON) see figures 2 - 7	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.



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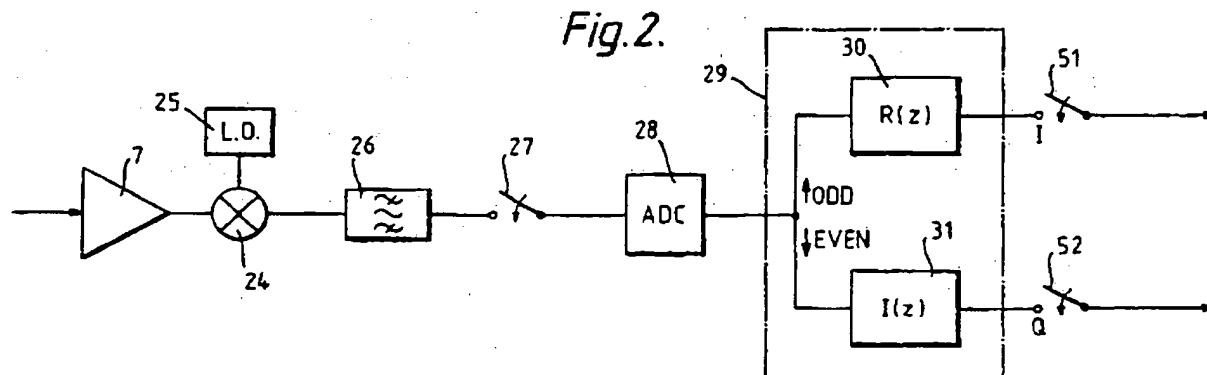
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Quadrature demodulator.

A quadrature demodulator for deriving an in-phase (I) and quadrature (Q) component from an input RF signal comprises means (24,25) for down-converting the RF signal to an IF signal. The IF signal is sampled (27) and digitised by an ADC (28). A complex digital filter (29) is used as a phase splitter designed to pass the positive IF frequency $+f_o$ but block the negative IF frequency $-f_o$. The resultant complex signal is in IQ form. By using four times oversampling at the ADC (28) the digital filter (29) can be split cleanly into two smaller filter sections (30, 31). By using feedforward filters for both these filter sections (30 and 31) a high degree of phase linearity can be achieved with minimal distortion.



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This invention relates to a demodulating arrangement for deriving an in-phase (I) and quadrature (Q) output signal from an input radio frequency (RF) signal.

In the field of RF communications it is sometimes required to obtain the base-band signal in a form having I and Q components. For example, the Pan-European Digital Mobile Communications system currently proposed by GSM employs gaussian minimum shift keying (GMSK) modulation. In this case IQ representation is necessary because the GMSK spectrum is asymmetric about the carrier.

A typical radio receiver front end configuration employing a conventional prior art quadrature demodulator is shown in Figure 1. The RF signal is received by an antenna 1. A duplexer 2 coupled to the antenna 1 passes the receive-band and rejects the transmit band. After low noise amplification at amplifier 3 the signal is then applied to a mixer 4 which mixes the signal down to a fixed intermediate frequency (IF), suitably 45MHz. To this end a locally generated signal having a predetermined frequency is applied to the mixer 4 from frequency synthesizer 5. The output signal is applied to a band pass filter 6 to isolate the required channel. At this stage the swing of the fading envelope is removed or attenuated by a limiter 7 or by automatic gain control. This measure is necessary in order to utilise the whole dynamic range of the analogue to digital converters (ADCs) used subsequently as much and as often as possible.

The base-band signal is obtained in IQ form using a conventional quadrature demodulator. The I and Q channels are obtained in two respective limbs of the demodulation circuit using a respective mixer 10, 11 and local oscillator 8, 9 where the signal from local oscillator 9 is phase shifted by 90° with respect to the signal from local oscillator 8. The I and Q channels are separately filtered at filters 12 and 13 respectively, sampled at 14 and 15, and then digitised by ADCs 16 and 17 with, for example, 8 bit resolution (this precision level can be reduced if limiting is always maintained).

The conventional quadrature demodulator described above suffers from the drawback that it is susceptible to imbalances between the non-ideal mixers, filters, samplers and ADCs in the two separate limbs of the circuit associated with the I and Q channels respectively.

With a view to overcoming the problems associated with the conventional quadrature demodulator, the article in 1984 IEEE Communications, pages 821-824 by Charles M. Rader proposes an alternative configuration employing a combination of mixing to a very low IF frequency, sampling and digitising, and then using digital filtering. The complex digital filter used comprises a pair of feedback filter sections associated respectively with the I and Q channels. This so-called infinite impulse response (IIR) filter thus acts as a digital phase splitter. IIRs do however have the drawback that the phase response is non-linear and can suffer distortion.

According to the present invention there is provided a demodulating arrangement for deriving an in-phase (I) and quadrature (Q) output signal from an input radio frequency (RF) signal, comprising RF signal input means, means for down-converting said RF signal to an intermediate frequency (IF) signal, means for sampling said IF signal, means for digitising the sampled signal, digital filter means comprising two feedforward filter sections, and means for applying the digitised signal sample selectively to the two sections of said digital filter means whereby I and Q signals are output from the two filter sections respectively.

It is noted that, as used herein, the term demodulating relates to the technique of deriving in-phase and quadrature samples from an RF input signal and the term quadrature demodulator is used accordingly.

Compared with the conventional quadrature demodulator described above, an arrangement in accordance with the present invention has the advantage that only a single mixer, filter and ADC are employed at the phase splitting and sampling stage. By halving the component count the power consumption can also be significantly reduced. Furthermore, the problem of matching gain and phase response between two components is avoided, since only a single mixer, filter, sampler and ADC need to be utilised. Moreover, in contrast with the arrangement disclosed in the IEEE article cited above, the use of a feedforward filter, specifically a so-called finite impulse response (FIR) filter, enables the filter to have a substantially linear phase response and to be substantially free from phase distortion.

Suitably the digital filter means is adapted to pass a band of frequencies including the positive frequency corresponding to the frequency of the IF signal and to attenuate a band of frequencies including the negative frequency corresponding to the frequency of the IF signal. In this case the result is a complex signal and the complex digital filter can be divided into a real part and an imaginary part corresponding to the I and Q signals respectively.

Preferably the digital filter means is adapted to pass a band of frequencies substantially centred on the positive frequency corresponding to the frequency of the IF signal and to attenuate a band of frequencies substantially centred on the negative frequency corresponding to the frequency of the IF signal.

In a preferred embodiment the sampling means is adapted to sample the IF signal at an integral multiple of four times the data symbol transmission rate. In this case the digital filter means splits cleanly

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into two feedforward filter sections.

As is usual, the term data symbol transmission rate used herein means the number of data symbols transmitted per unit time from the transmitter, which value is assumed to be known by the receiver.

An embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings, in which

Figure 1 is a schematic circuit diagram of a radio receiver front end comprising a prior art quadrature demodulator,

Figure 2 is a schematic circuit diagram of a quadrature demodulating arrangement in accordance with the invention,

Figure 3a shows the frequency response of a digital filter,

Figure 3b shows the frequency-translated response of the digital filter used in the circuit of Figure 2, and

Figures 4a and 4b are block schematic diagrams of filter sections used in the circuit of Figure 2.

The quadrature demodulating arrangement shown in Figure 2 may be incorporated in a radio receiver front end similar to that illustrated in Figure 1.

In this case however the IF output of AGC/limiter stage 7 is further down-converted at a second mixer stage 24 to a second intermediate frequency, by mixing with a signal of predetermined frequency from a local oscillator 25. Any suitable value may be selected for the first IF frequency, depending on the desired second IF and mixer stage requirements. The frequency f_o of the second IF may be selected to be an integral multiple of the data symbol transmission rate f_s , i.e.

$$f_o = n f_s,$$

where $n = 1, 2, 3, \dots$

However, it has to be noted that in the case where GMSK is used (e.g. for a receiver compatible with the GSM Digital Mobile system as mentioned above) the second IF f_o is chosen in accordance with the formula

$$f_o = (n - \frac{1}{2}) f_s,$$

again where $n = 1, 2, 3, \dots$, and f_s is the data symbol transmission rate. The negative offset in the second IF, equivalent to $\frac{1}{2} f_s$ is required to facilitate demodulation in this case.

In the present (non-GSM) embodiment, however, the second IF frequency f_o is chosen to be equal to the data symbol transmission rate f_s , i.e. $f_o = f_s$.

The second IF signal output from mixer 24 is filtered by bandpass filter 26 and subsequently sampled by the sampler 27 and digitised by the ADC 28. The sampling rate is selected to be a factor of four times the data symbol transmission rate. Thus, for example four or eight times oversampling may be used. The resolution of ADC 28 may, for example, be 8 bits. In the present embodiment four times oversampling is used.

The output from ADC 28 is then applied to a complex digital filter 29. The filter 29 is a so-called finite impulse response (FIR) filter comprising $R(z)$ as its real part 30 and $I(z)$ as its imaginary part 31.

As is well-known when a real signal is down-converted to an IF frequency f_o , the resultant signal also has an image centred on $-f_o$. The principle of digital phase splitting employed in the present invention involves using as the complex digital filter 29 a real low-pass FIR and arranging that the passband coincides with the $+f_o$ image, but blocks the image at $-f_o$, resulting in a complex signal output, as will now be explained.

Figure 3a shows the frequency response of a general FIR filter. The pass band is centred on $\omega T = 0$, where T is the sampling period and ω is the angular frequency. The transfer function of the filter in the z domain, $H(z)$, is given by

$$H(z) = \sum_{i=0}^N a_i z^{-i}$$

Translating this into the ω (frequency) domain i.e.

$$H(z) \rightarrow H(e^{j\omega T})$$

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$$H(e^{j\omega T}) = \sum_{i=0}^n a_i e^{-j\omega T i}$$

5

Generally, the frequency response can be translated from ω to ω' by an amount ω_0 , i.e.

$$\omega' = \omega + \omega_0$$

$$\text{Therefore, } \omega = (\omega' - \omega_0)$$

10

Hence

15

$$H(e^{j(\omega' - \omega_0)T}) = \sum_{i=0}^n a_i e^{-j(\omega' - \omega_0)T i}$$

$$= \sum a_i e^{j\omega_0 T i} e^{-j\omega' T i}$$

20

Therefore, the new z transform $H'(z)$ of the frequency-translated filter is:

25

$$H'(z) = \sum_{i=0}^n a_i e^{j\omega_0 T i} z^{-i} \dots\dots\dots (1)$$

It can thus be seen that each term of $H(z)$ is modified by the factor $e^{j\omega_0 T i}$.

30

Now, $T = 1/(f_{ADC})$

where f_{ADC} is the sampling rate at the ADC 28. If four times oversampling is used then

$$f_{ADC} = 4f_0$$

35

$$\text{Therefore } T = 1/(4f_0) \quad (2)$$

If the frequency translation is chosen to be equal to a quarter of the ADC sampling rate, i.e. $(f_{ADC}/4) = f_0$, then

40

$$\omega_0 = 2\pi f_0 \quad (3)$$

Substituting equations (2) and (3) into equation (1), we have

45

$$H'(z) = \sum a_i e^{j\pi i/2} z^{-i} \quad (4)$$

50

Figure 3b shows the frequency-translated spectrum 61 of the filter $H'(z)$, in this particular case where the frequency translation is chosen to be equal to a quarter of the ADC sampling rate. It can be seen that the maximum frequency response now occurs at $\pi/2$ corresponding to a frequency $+f_0$. Figure 3b also shows the $+f_0$ spectral component 62 and the $-f_0$ spectral component 63 of the RF signal. Only the $+f_0$ component 62 is within the filter spectrum 61. In other words the pass band coincides with the $+f_0$ image, but the filter blocks the $-f_0$ image.

Referring back to equation (4) the terms of the summation fall alternately into real and imaginary values,

55

as follows:

The first term, when $i = 0$, is

$$a_0 e^{j0} z^{-0} = a_0$$

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The second term, when $i = 1$, is:

$$a_1 e^{j\pi/2} z^{-1} = j a_1 z^{-1}$$

5

The third term, when $i = 2$, is:

$$a_2 e^{j\pi} z^{-2} = -a_2 z^{-2}$$

10 The fourth term, when $i = 3$, is:

$$a_3 e^{j3\pi/2} z^{-3} = -ja_3 z^{-3}$$

The fifth term, when $i = 4$, is:

15

$$a_4 e^{j2\pi} z^{-4} = a_4 z^{-4}$$

and so on for succeeding terms.

Thus it can be seen that the even terms have pure real values, and the odd terms have pure imaginary values. In this particular case (i.e. where the frequency response is shifted by a quarter of the ADC sampling rate), the digital filter splits cleanly into two distinct (smaller) feedforward filter sections 30, 31 associated respectively with real and imaginary parts $R(z)$ and $I(z)$, see Figure 2. The structure of the filter sections 30 and 31 is discussed in more detail below with reference to Figures 4a and 4b.

It is evident from the foregoing analysis that when the filter output is downsampled by 2^n only odd samples are needed for calculating Q and only even samples are needed for calculating I . Therefore only the even samples are applied to feedforward filter section 30 and the odd samples are applied to feedforward filter section 31, as indicated in Figure 2.

The Applicant has used a fifteenth order FIR 29 comprising eight taps in the feedforward filter section 30 and seven taps in the feedforward filter section 31 as shown in Figures 4a and 4b respectively and discussed in more detail below. Depending on specific design circumstances the two filter sections may comprise more or less taps.

The desired I and Q signals are obtained by sampling the output of filter sections 30 and 31 at samplers 51 and 52 respectively. In the specific embodiment described here four times downsampling is preferably used, i.e. the output sampling rate is equal to the IF frequency $f_o = (f_{\text{ADC}}/4)$. In this case the complex signal is automatically output in IQ form. Alternative final sampling rates may be used as mentioned above, i.e. downsampling by 2^n , but then further calculation may be required. For example, in the case of two times downsampling (i.e. final sampling rate $= 2f_o$) each sample is rotated by π and therefore alternate samples would have to be sign reversed to recover the I and Q components. In general, if the IF frequency f_o is an integral multiple of the final sampling rate at samplers 51 and 52 then no sign reversal is necessary.

Referring now to Figure 4a, the feedforward filter section 30 comprises a transversal filter formed by a tapped delay line 32 comprising eight taps which are connected to respective multipliers 33 to 40 in which the signals derived are multiplied by respective weighting factors W_0 to W_7 . In a specific embodiment the Applicant has used the following weighting coefficients quantized to 8 bits precision, viz. $W_0 = 4$, $W_1 = 0$, $W_2 = -12$, $W_3 = -72$, $W_4 = 72$, $W_5 = 12$, $W_6 = 0$, $W_7 = -4$. The multiplier outputs are summed in an addition stage 41, the output of which constitutes the I form of the signal.

Referring to Figure 4b, the feedforward filter section 31 similarly comprises a transversal filter 42 formed by a tapped delay line 42 comprising seven taps connected to respective multipliers 43 to 49 in which the signals derived are multiplied by respective weighting factors W_8 to W_{14} . In conjunction with the specific weighting factors quoted above for the filter section 30, the Applicant has used the following weighting coefficients quantized to 8 bits precision, viz. $W_8 = 8$, $W_9 = 14$, $W_{10} = 22$, $W_{11} = 96$, $W_{12} = 22$, $W_{13} = 22$, $W_{14} = 14$, $W_{15} = 8$. The multiplier outputs are summed in an addition stage 50, the output of which constitutes the Q form of the signal.

In view of the foregoing, it will be evident to a person skilled in the art that various modifications may be made within the scope of the present invention. For example the various sampling rates may be selected according to particular circumstances and requirements. Furthermore the two feedforward filter sections may comprise fewer or more than fifteen taps depending on the specific filter characteristic (frequency response) desired. Also, the two filter sections may comprise an equal number of taps, or the filter s ction

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31 may comprise an odd number of taps while the filter section 30 has an even number.

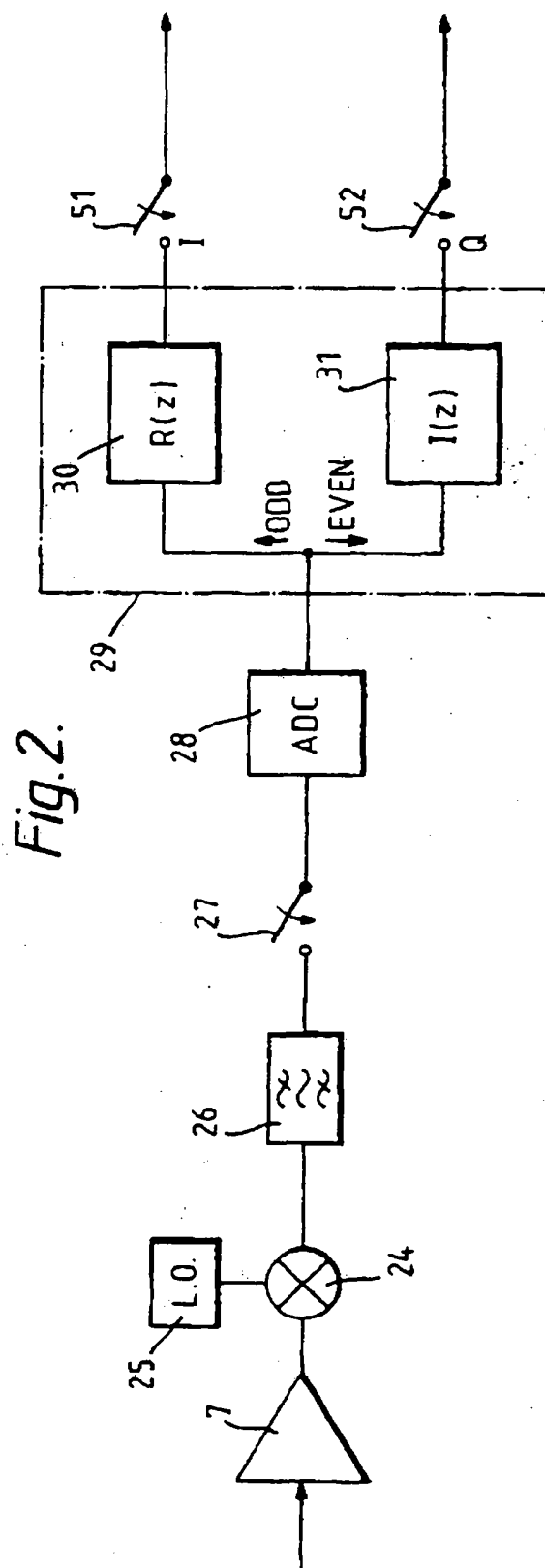
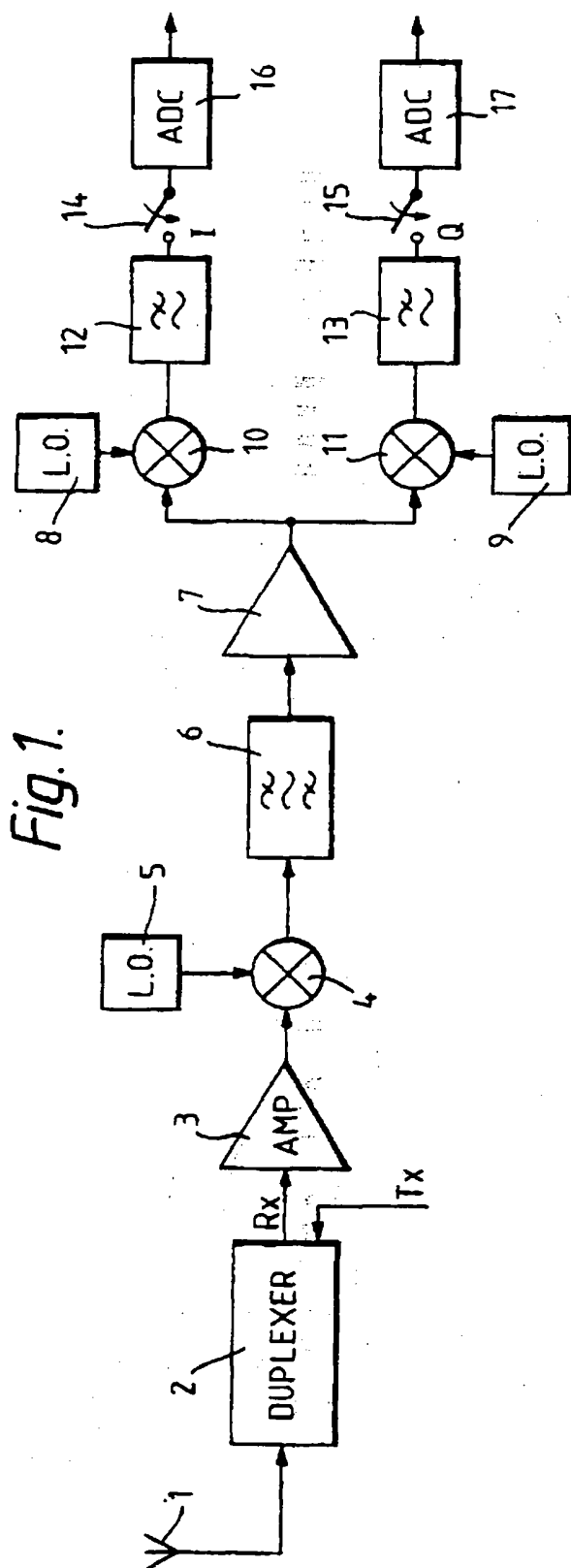
Claims

- 5 1. A demodulating arrangement for deriving an in-phase (I) and quadrature (Q) output signal from an input radio frequency (RF) signal, comprising
RF signal input means,
means for down-converting said RF signal to an intermediate frequency (IF) signal,
means for sampling said IF signal,
10 means for digitising the sampled signal,
digital filter means comprising two feedforward filter sections, and
means for applying the digitised signal sample selectively to the two sections of said digital filter means whereby I and Q signals are output from the two filter sections respectively.
- 15 2. A demodulating arrangement as claimed in claim 1, wherein the digital filter means is adapted to pass a band of frequencies including the positive value of frequency ($+f_0$) corresponding to the frequency (f_0) of the IF signal and to attenuate a band of frequencies including the negative value of frequency ($-f_0$) corresponding to the frequency (f_0) of the IF signal.
- 20 3. A demodulating arrangement as claimed in claim 2, wherein the digital filter means is adapted to pass a band of frequencies substantially centred on the positive value of frequency ($+f_0$) corresponding to the frequency (f_0) of the IF signal and to attenuate a band of frequencies substantially centred on the negative value of frequency ($-f_0$) corresponding to the frequency (f_0) of the IF signal.
- 25 4. A demodulating arrangement as claimed in any of the preceding claims, wherein the sampling means is adapted to sample the IF signal at an integral multiple of four times the data symbol transmission rate.
5. A demodulating arrangement as claimed in any of the preceding claims, including means for sampling the output from the two feedforward filter sections at a rate substantially equal to an integral multiple of
30 the IF frequency (f_0).
6. A demodulating arrangement as claimed in any of the preceding claims, wherein the two sections of the digital filter means each comprise a tapped delay line, having an unequal number of taps in each section.
- 35 7. A demodulating arrangement as claimed in claim 6, wherein one of the two sections of said digital filter means has one more tap than the other of the two sections of said filter means.
8. A demodulating arrangement as claimed in any of the preceding claims, wherein the down converting means is adapted to down-convert the RF signal to an intermediate frequency the value of which is an
40 integral multiple of the data symbol transmission rate.
9. A demodulating arrangement as claimed in claim 8, wherein the down-converting means is adapted to down-convert the RF signal to an intermediate frequency the value of which is equal to the data symbol
45 transmission rate.
10. A demodulating arrangement as claimed in any of claims 1 to 8, wherein the down-converting means is adapted to down-convert the RF signal to an intermediate frequency the value of which is a factor of $(n-\frac{1}{4})$ times the data symbol transmission rate, where n is an integer.

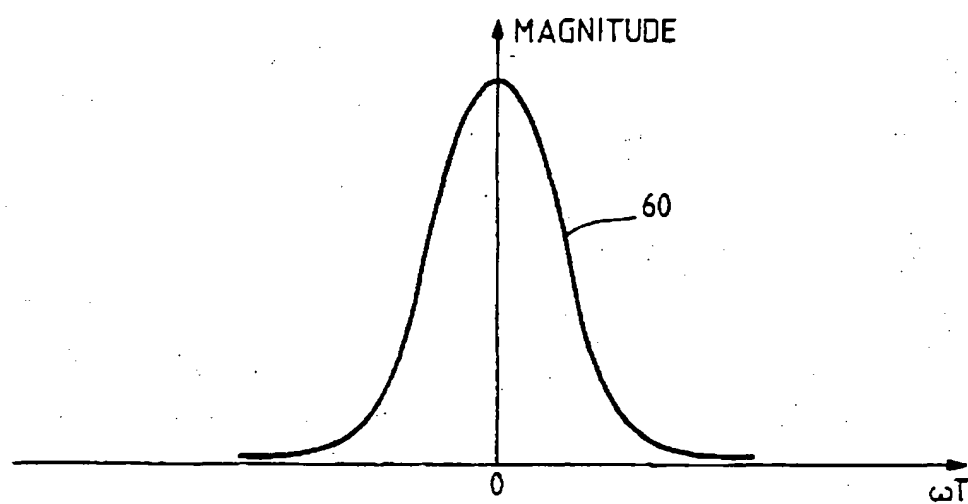
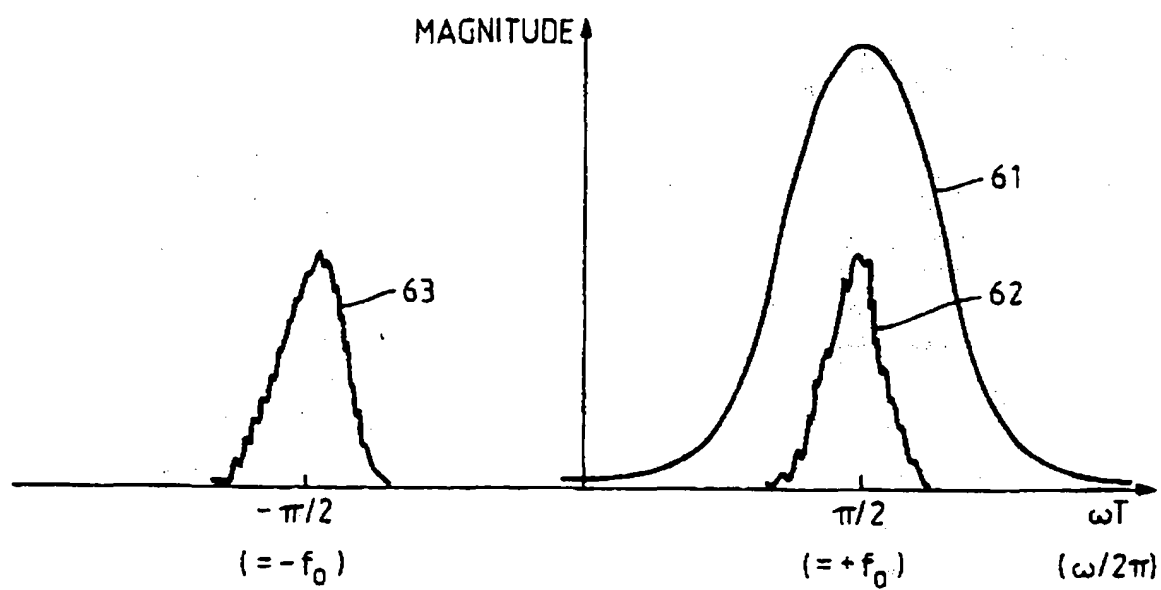
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Fig. 3a.*Fig. 3b.*

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Fig. 4a.

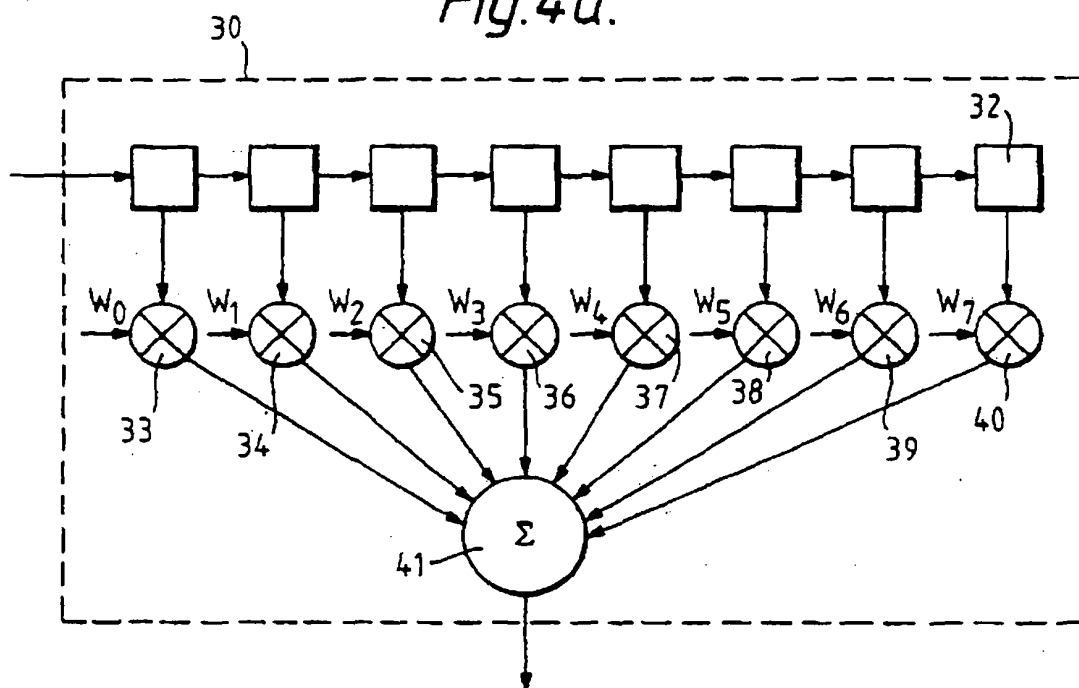
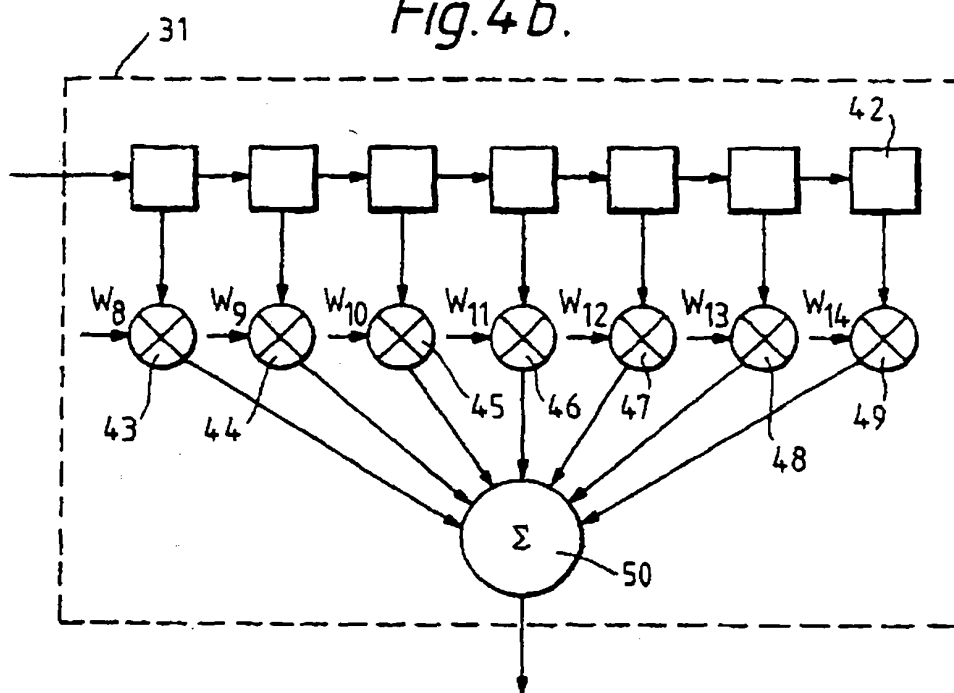


Fig. 4b.



(19)



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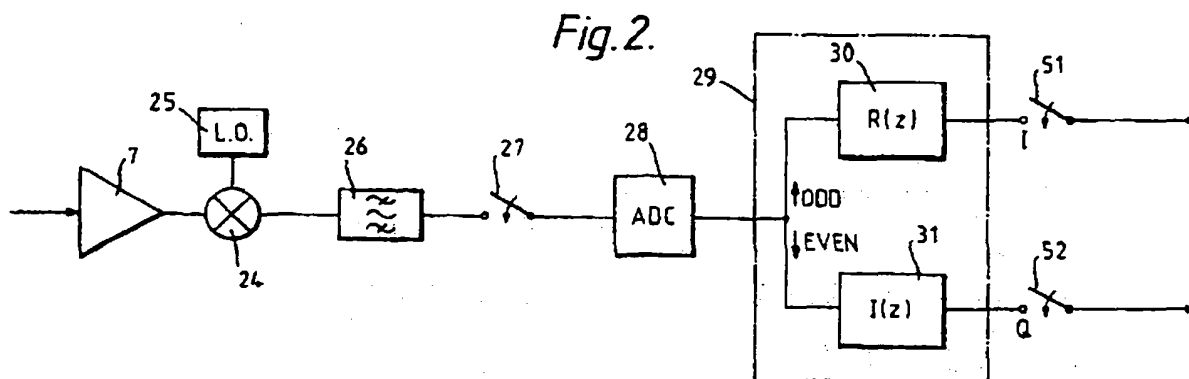
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27.11.91 Bulletin 91/48(84) Designated Contracting States:
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18.12.91 Bulletin 91/51(71) Applicant: **TECHNOPHONE LIMITED**
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Technophone Limited Intellectual Property
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Camberley, Surrey GU15 3SP(GB)(54) **Quadrature demodulator.**

(57) A quadrature demodulator for deriving an in-phase (I) and quadrature (Q) component from an input RF signal comprises means (24,25) for down-converting the RF signal to an IF signal. The IF signal is sampled (27) and digitised by an ADC (28). A complex digital filter (29) is used as a phase splitter designed to pass the positive IF frequency $+f_0$ but block the negative IF frequency $-f_0$. The

resultant complex signal is in IQ form. By using four times oversampling at the ADC (28) the digital filter (29) can be split cleanly into two smaller filter sections (30, 31). By using feedforward filters for both these filter sections (30 and 31) a high degree of phase linearity can be achieved with minimal distortion.

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European Patent
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EUROPEAN SEARCH REPORT

Application Number

EP 91 30 3193

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US-A-4 779 054 (MONTELEONE ET AL.) " column 1, line 64 - column 4, line 15; figures 1, 2 "	1, 5	H0301/22 H04L27/22
Y	---	4, 8	
X	US-A-4 737 728 (NAKAMURA ET AL.) " column 2, line 42 - column 7, line 6; figures 1-4 "	1-3	
Y	---	4, 8	
Y	US-A-4 849 991 (ARNOLD ET AL.) " column 5, line 38 - column 6, line 10; figure 2 "	4, 8	
A, D	IEEE TRANSACTIONS ON AEROSPACE AND ELECTRONIC SYSTEMS vol. 30, no. 6, November 1984, NEW YORK, US pages 821 - 824; RADER, C.M.: 'A SIMPLE METHOD FOR SAMPLING IN-PHASE AND QUADRATURE COMPONENTS' " the whole document "	1	
E	EP-A-0 428 226 (PHILIPS PATENTVERWALTUNG GMBH) " the whole document "	1, 8, 9	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H03D H04L
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 16 OCTOBER 1991	Examiner BALBINOT H.
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application I : document cited for other reasons & : member of the same patent family, corresponding document</p>			